Serial Interface Module Functional Specification

ST-5211   ST-5212
ST-5221   ST-5231
ST-5232
ST-5252   ST-5272

User Manual

Version 1.05

2013 CREVIS Co.,Ltd

DOCUMENT CHANGE SUMMARY				
REV	PAGE	REMARKS	DATE	EDITOR
1.0	New Document	Draft	2010/12/6	JE KANG
1.01	21	Delete *Note 1	2011/12/15	JE KANG
1.02	6 19, 23	Add your experience Delete : Configuration Parameter Data Byte#0, 5bit-> 9 Bata bit Add ST-5252, ST-5272 (Coming Soon)	2012/1/13	JE KANG
1.03		Changed Crevis TEL	2013/4/4	JE KANG
1.04		Environment Spec. 50℃→55℃ (UL Temp)	2013/7/3	JE KANG
1.05		Changed Power Dissipation "ST-5252, ST-5272"	2013/7/17	JE KANG

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1. Important Notes

Solid state equipment has operational characteristics differing from those of electromechanical equipment.

Safety Guidelines for the Application, Installation and Maintenance of Solid State Controls describes some important differences between solid state equipment and hard-wired electromechanical devices.

Because of this difference, and also because of the wide variety of uses for solid state equipment, all persons responsible for applying this equipment must satisfy themselves that each intended application of this equipment is acceptable.

In no event will CREVIS be responsible or liable for indirect or consequential damages resulting from the use or application of this equipment.

The examples and diagrams in this manual are included solely for illustrative purposes. Because of the many variables and requirements associated with any particular installation, CREVIS cannot assume responsibility or liability for actual use based on the examples and diagrams.

Warning!

✓ **If you don't follow the directions, it could cause a personal injury, damage to the equipment or explosion**

● Do not assemble the products and wire with power applied to the system. Else it may cause an electric arc, which can result into unexpected and potentially dangerous action by field devices. Arching is explosion risk in hazardous locations. Be sure that the area is non-hazardous or remove system power appropriately before assembling or wiring the modules.

● Do not touch any terminal blocks or IO modules when system is running. Else it may cause the unit to an electric shock or malfunction.

● Keep away from the strange metallic materials not related to the unit and wiring works should be controlled by the electric expert engineer. Else it may cause the unit to a fire, electric shock or malfunction.

Caution!

✓ **If you disobey the instructions, there may be possibility of personal injury, damage to equipment or explosion. Please follow below Instructions.**

● Check the rated voltage and terminal array before wiring. Avoid the circumstances over 55℃ of temperature. Avoid placing it directly in the sunlight.

● Avoid the place under circumstances over 85% of humidity.

● Do not place Modules near by the inflammable material. Else it may cause a fire.

● Do not permit any vibration approaching it directly.

● Go through module specification carefully, ensure inputs, output connections are made with the specifications. Use standard cables for wiring.

● Use Product under pollution degree 2 environment.

1.1 Safety Instruction

1.1.1 Symbols

DANGER	Identifies information about practices or circumstances that can cause an explosion in a hazardous environment, which may lead to personal injury or death property damage, or economic loss
IMPORTANT	Identifies information that is critical for successful application and understanding of the product
ATTENTION	Identifies information about practices or circumstances that can lead to personal injury, property damage, or economic loss. Attentions help you to identity a hazard, avoid a hazard, and recognize the consequences

1.1.2 Safety Notes

DANGER	The modules are equipped with electronic components that may be destroyed by electrostatic discharge. When handling the modules, ensure that the environment (persons, workplace and packing) is well grounded. Avoid touching conductive components, e.g. FnBUS Pin.

1.1.3 Certification

c-UL-us UL Listed Industrial Control Equipment, certified for U.S. and Canada

See UL File E235505

DNV CERTIFICATE No. A-10666

CE Certificate

EN 61000-6-2; Industrial Immunity

EN 61000-6-4; Industrial Emissions

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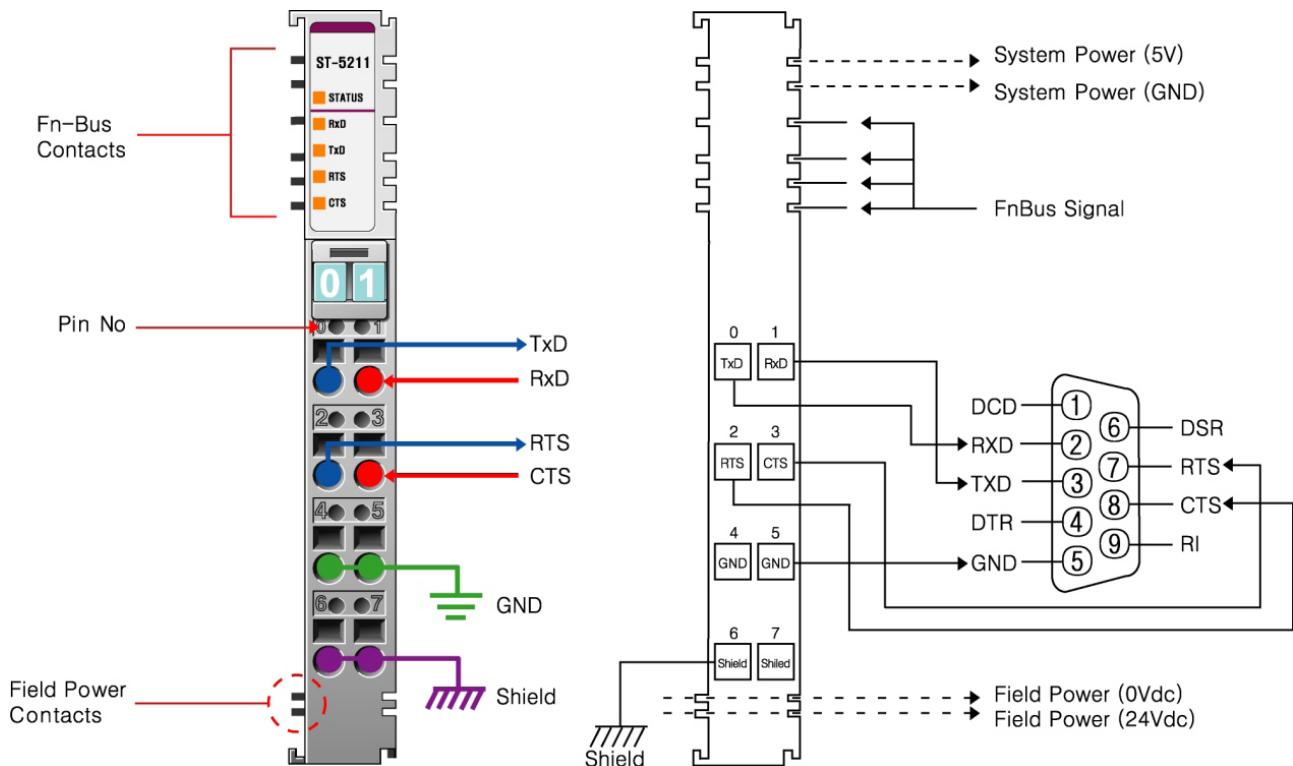
2. SERIAL MODULE LIST

ST-Number	Description	Catalog Number(hex)	Product Code(hex)
ST-5211	RS232 Communication, 1Channel, RTS/CTS Flow Control	42 05 05 C1	05 05 D0 01
ST-5212	RS232 Communication, 2Channel	43 0B 0B C1	0B 0B D0 01
ST-5221	RS422 Communication, 1Channel	44 05 05 C1	05 05 D0 01
ST-5231	RS485 Communication, 1Channel	45 05 05 C1	05 05 D0 01
ST-5232	RS485 Communication, 2Channel	46 0B 0B C1	0B 0B D0 01
ST-5252	RS232 Communication, 2Channel, Premium Type	Coming Soon	Coming Soon
ST-5272	RS485 Communication, 2Channel, Premium Type	Coming Soon	Coming Soon

3. Specification

3.1 The Interface
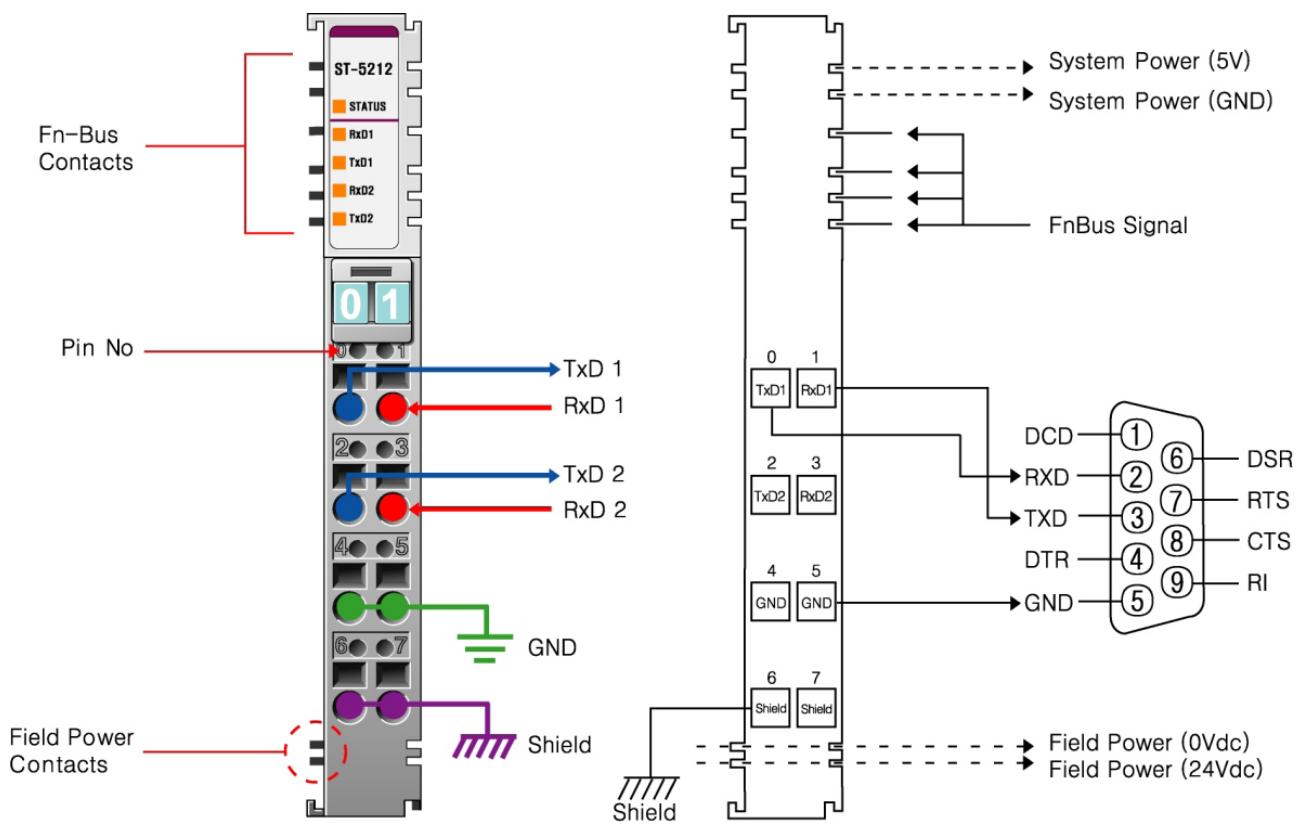
3.1.1 ST-5211(RS232/1channel)

Pin No.	Description	Pin No.	Description
0	TxD	1	RxD
2	RTS	3	CTS
4	GND	5	GND
6	SHIELD	7	SHIELD

LED NAME	COLOR	STATUS
RxD	Green	Received Data
TxD	Green	Transmit Data
RTS	Green	Request-to-send
CTS	Green	Clear-to-send
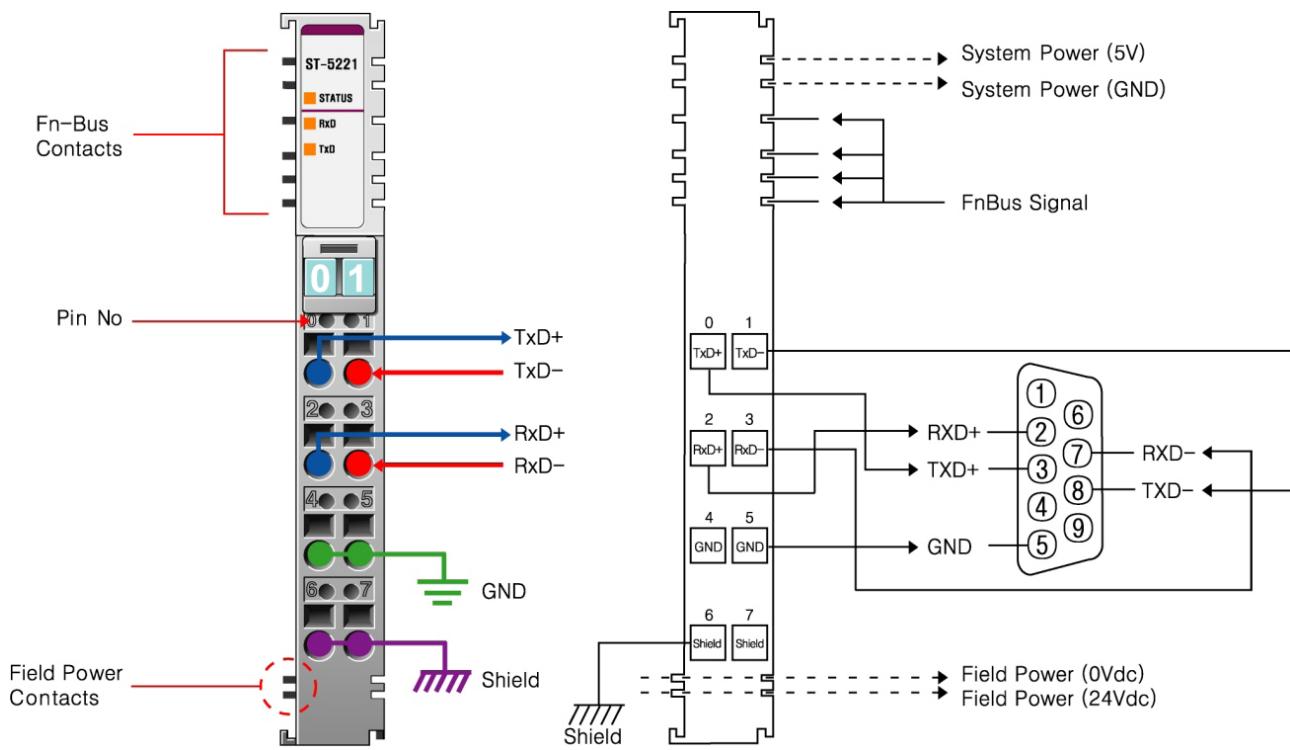
3.1.2 ST-5212(RS232/2channel)

Pin No.	Description	Pin No.	Description
0	TxD1 channel #0	1	RxD1 channel #0
2	TxD2 channel #1	3	RxD2 channel #1
4	GND	5	GND
6	SHIELD	7	SHIELD
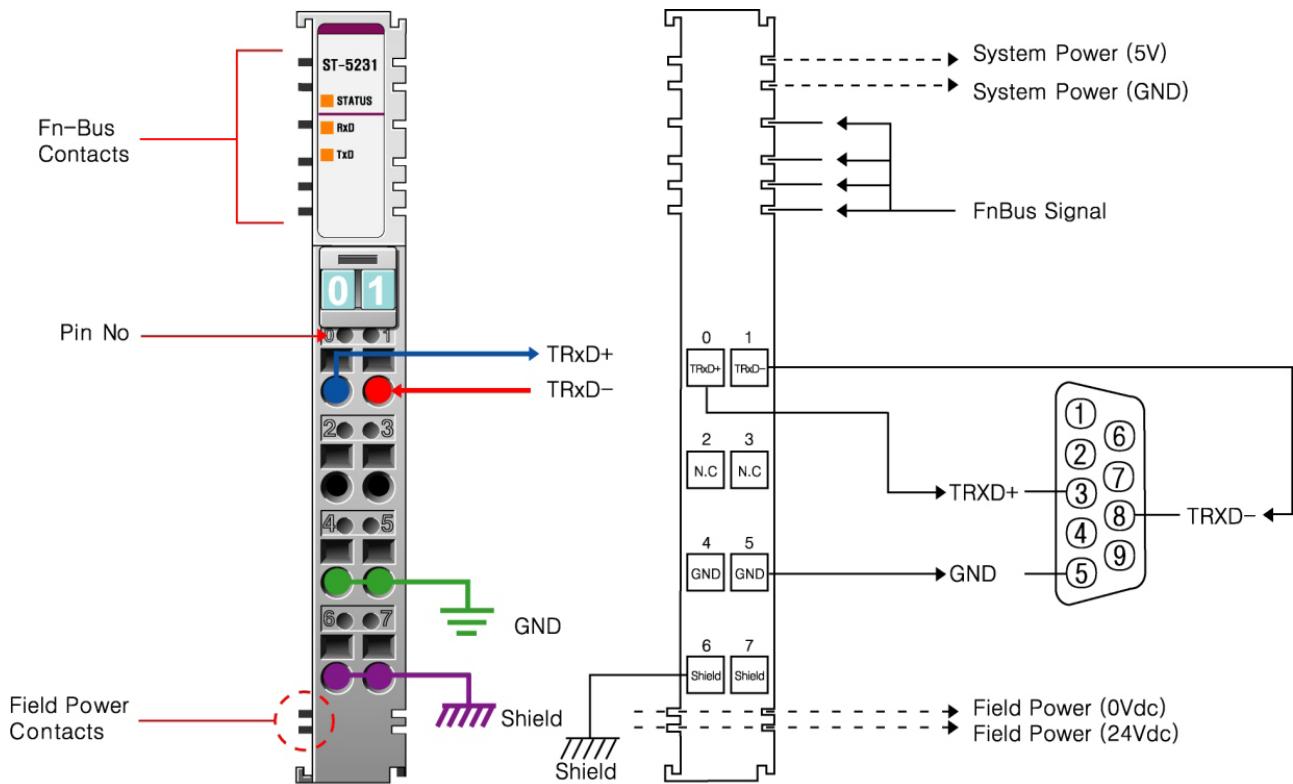
LED NAME	COLOR	STATUS
RxD1	Green	Received Data #0
TxD1	Green	Transmit Data #0
RxD2	Green	Received Data #1
TxD2	Green	Transmit Data #1

3.1.3 ST-5221(RS422/1channel)

Pin No.	Description	Pin No.	Description
0	TxD +	1	TxD -
2	RxD +	3	RxD -
4	GND	5	GND
6	SHIELD	7	SHIELD

LED NAME	COLOR	STATUS
RxD	Green	Received Data
TxD	Green	Transmit Data
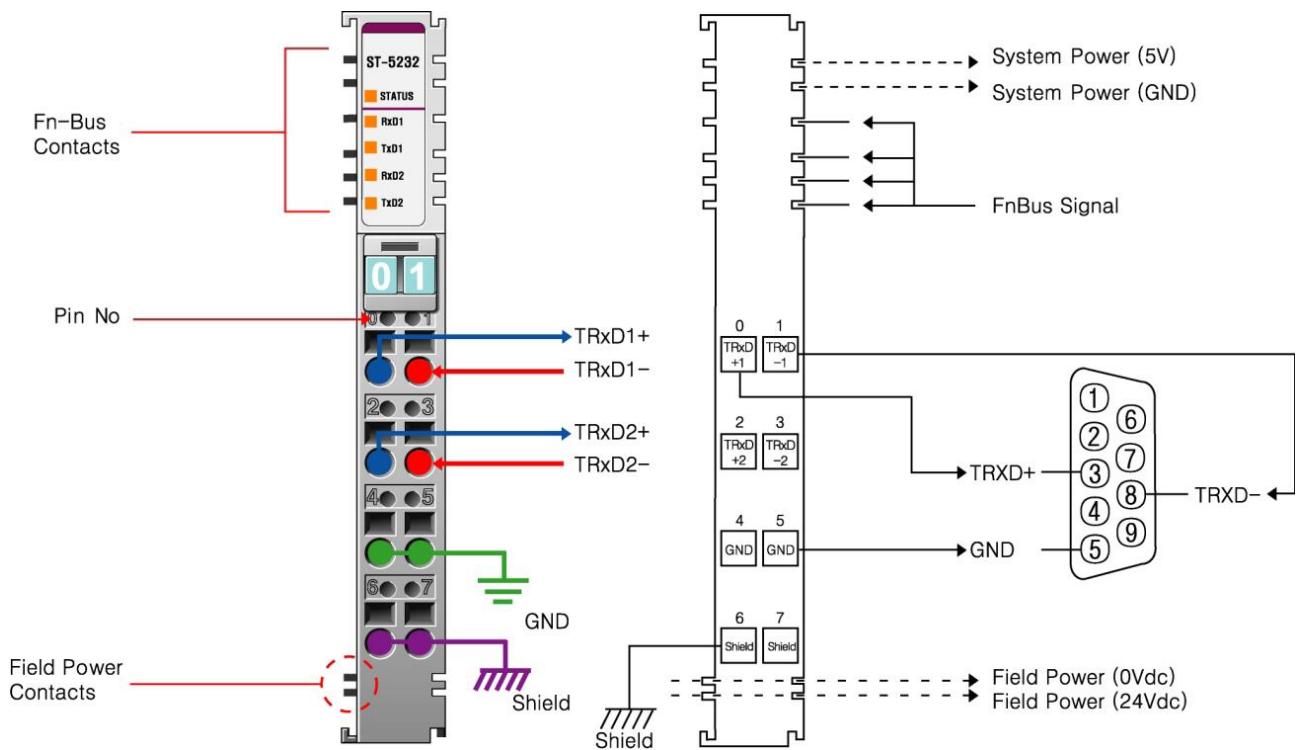
3.1.4 ST-5231(RS485/1channel)

Pin No.	Description	Pin No.	Description
0	RS 485 +	1	RS 485 -
2	--	3	--
4	GND	5	GND
6	SHIELD	7	SHIELD

LED NAME	COLOR	STATUS
RxD	Green	Received Data
TxD	Green	Transmit Data
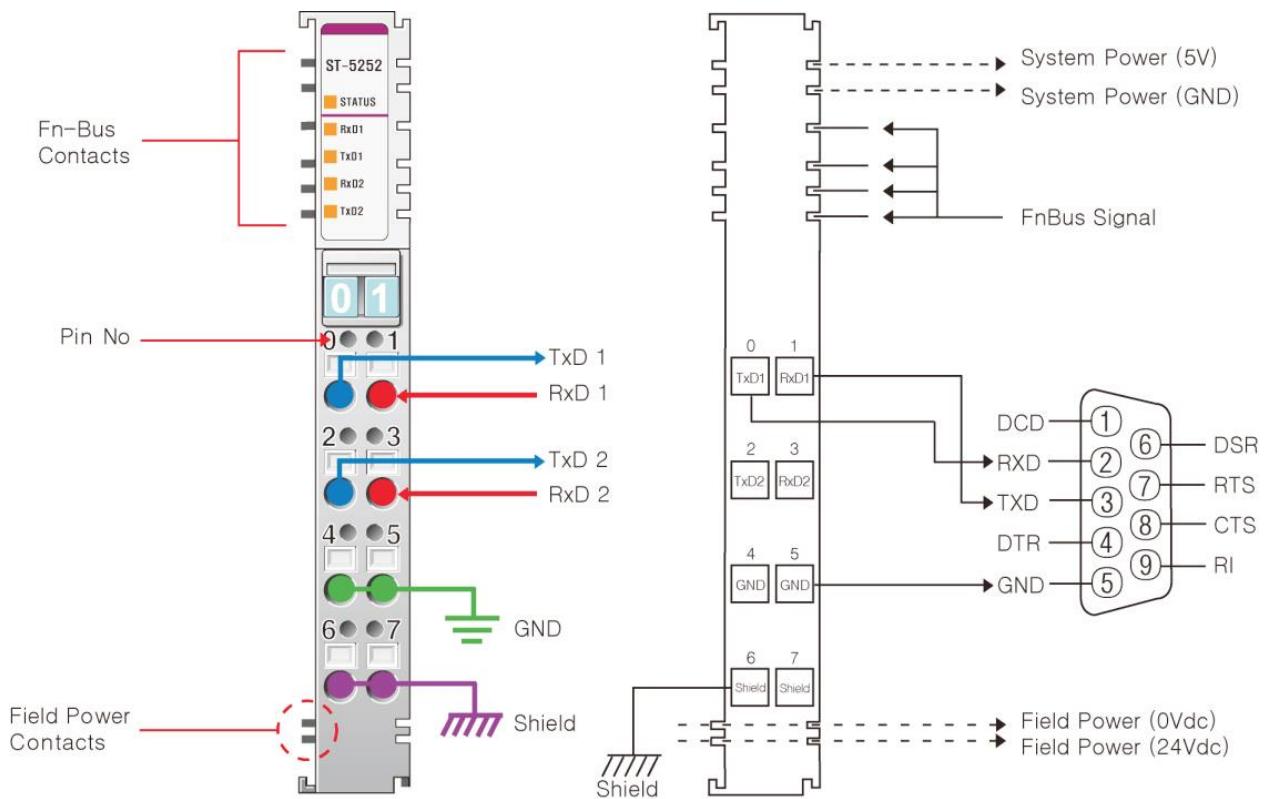
3.1.5 ST-5232 (RS485/2channel)

Pin No.	Description	Pin No.	Description
0	RS485 + Channel #0	1	RS485 - Channel #0
2	RS485 + Channel #1	3	RS485 - Channel #1
4	GND	5	GND
6	SHIELD	7	SHIELD

LED NAME	COLOR	STATUS
RxD1	Green	Received Data #0
TxD1	Green	Transmit Data #0
RxD2	Green	Received Data #1
TxD2	Green	Transmit Data #1
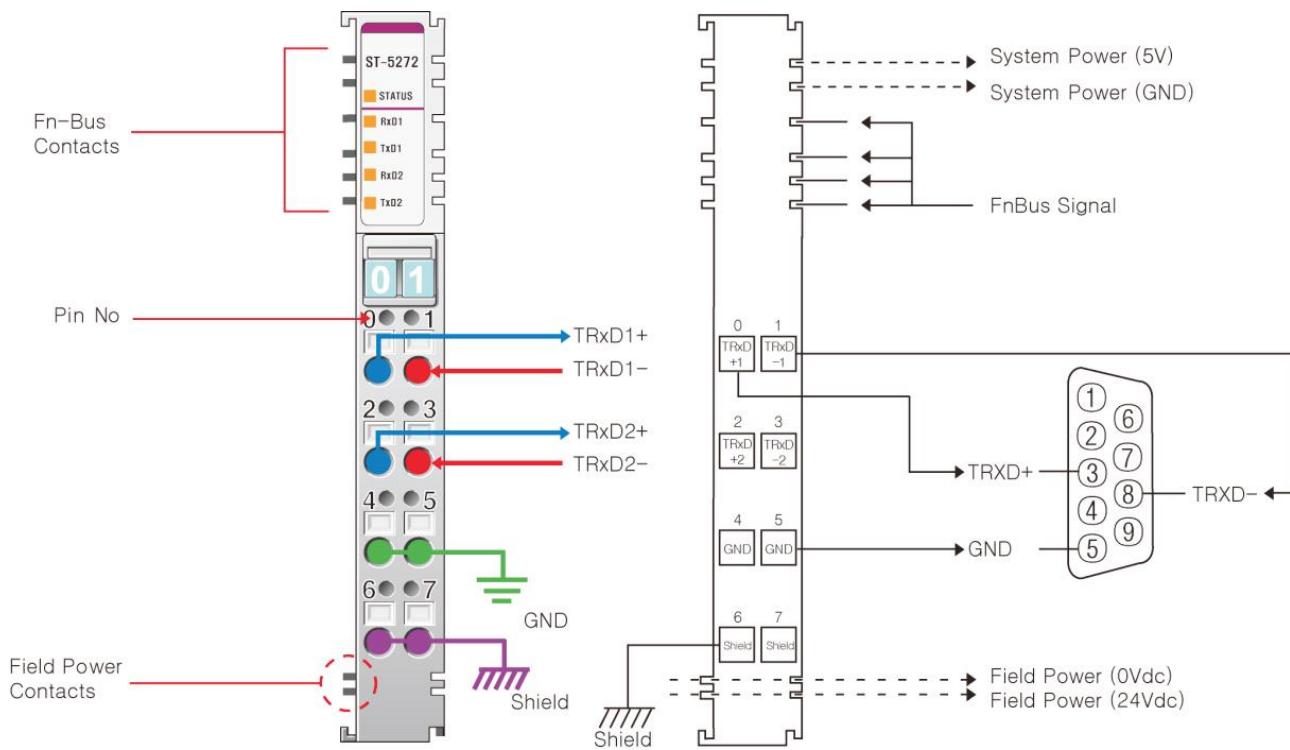
3.1.6 ST-5252(RS232/2channel/Premium Type)   Coming Soon

Pin No.	Description	Pin No.	Description
0	TxD1 channel #0	1	RxD1 channel #0
2	TxD2 channel #1	3	RxD2 channel #1
4	GND	5	GND
6	SHIELD	7	SHIELD

LED NAME	COLOR	STATUS
RxD1	Green	Received Data #0
TxD1	Green	Transmit Data #0
RxD2	Green	Received Data #1
TxD2	Green	Transmit Data #1

3.1.7 ST-5272 (RS485/2channel/Premium Type) Coming Soon

Pin No.	Description	Pin No.	Description
0	RS485 + Channel #0	1	RS485 - Channel #0
2	RS485 + Channel #1	3	RS485 - Channel #1
4	GND	5	GND
6	SHIELD	7	SHIELD

LED NAME	COLOR	STATUS
RxD1	Green	Received Data #0
TxD1	Green	Transmit Data #0
RxD2	Green	Received Data #1
TxD2	Green	Transmit Data #1

3.2 Specification

3.2.1. ST-5211, ST-5212, ST-5221, ST-5231, ST-5232

Items	ST-5211	ST-5212	ST-5221	ST-5231	ST-5232
Interface Specification					
Transfer Channels	TxD, RxD, Full duplex	TxD, RxD, Full duplex	TxD, RxD, Full duplex	TxD, RxD, Half duplex	TxD, RxD, Half duplex
Transfer Rate	300~115200	300~115200	300~115200	300~115200	300~115200
Data Bit	7bit, 8bit	7bit, 8bit	7bit, 8bit	7bit, 8bit	7bit, 8bit
Parity Bit	None, Odd, Even	None, Odd, Even	None, Odd, Even	None, Odd, Even	None, Odd, Even
Stop Bit	1bit, 2bit	1bit, 2bit	1bit, 2bit	1bit, 2bit	1bit, 2bit
Flow Control	RTS,CTS	--	RTS,CTS	RTS,CTS	--
Bit Distortion	<1.6%	<1.6%	<1.6%	<1.6%	<1.6%
Connection	Spring force of RTB	Spring force of RTB	Spring force of RTB	Spring force of RTB	Spring force of RTB
Cable Length	Max.15m	Max.15m	1km twisted pair	1km twisted pair	1km twisted pair
Low Signal Voltage	-18V~-3V	-18V~-3V	--	--	--
High Signal Voltage	+18V~+3V	+18V~+3V	--	--	--
Isolation	Isolation Voltage: 1000Vrms/Vac	Isolation Voltage: 1000Vrms/Vac	Isolation Voltage: 1000Vrms/Vac	Isolation Voltage: 1000Vrms/Vac	Isolation Voltage: 1000Vrms/Vac
RxD Buffer	1024Byte	1024Byte	1024Byte	1024Byte	1024Byte
TxD Buffer	256Byte	256Byte	256Byte	256Byte	256Byte
Line Impedance	--	--	120Ω	120Ω	120Ω
Input Image Size	6Byte	12Byte	6Byte	6Byte	12Byte
Output Image Size	6Byte	12Byte	6Byte	6Byte	12Byte
General Specification					
Power dissipation (System Power)	95mA max @ 5.0Vdc	110mA max @ 5.0Vdc	155mA max @ 5.0Vdc	110mA max @ 5.0Vdc	155mA max @ 5.0Vdc
Operating Temperature	-20℃~55℃	-20℃~55℃	-20℃~55℃	-20℃~55℃	-20℃~55℃
Non-Operating Temperature	-40℃~85℃	-40℃~85℃	-40℃~85℃	-40℃~85℃	-40℃~85℃
Relative Humidity	5%~95% Non-condensing	5%~95% Non-condensing	5%~95% Non-condensing	5%~95% Non-condensing	5%~95% Non-condensing
Operating Altitude	2000m	2000m	2000m	2000m	2000m
Shock Operating	30g	30g	30g	30g	30g
Shock Non-Operating	50g	50g	50g	50g	50g
Vibration	2g@10-500Hz	2g@10-500Hz	2g@10-500Hz	2g@10-500Hz	2g@10-500Hz
Module Size	12x70x99 (WxHxL)	12x70x99 (WxHxL)	12x70x99 (WxHxL)	12x70x99 (WxHxL)	12x70x99 (WxHxL)

Class 2, Adjacent to voltage rating (30Vmax)

Class 2, 24VDC

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3.2.2. ST-5252, ST-5272 (Premium Type)   Coming Soon

Items	Specification (ST-5252)	Specification(ST-5272)
Input Specification		
Transfer Channels	TxD, RxD, Full Duplex	TxD, RxD, Half Duplex
Transfer Rate	1,200~115,200bps (* default: 9,600bps)	1,200~115,200bps (* default: 9,600bps)
Data Bit	7bits, 8bits (* default : 8bits)	7bits, 8bits (* default : 8bits)
Parity Bit	None, Odd, Even (*default : None)	None, Odd, Even (*default : None)
Stop Bit	1bit, 2bits (*default : 1bit)	1bit, 2bits (*default : 1bit)
Bit Distortion	<1.6%	<1.6%
Connection	Spring force of RTB	Spring force of RTB
Cable Length	Max. 15m	1Km twisted pair
Low Signal Voltage	-18V ~ -3V	--
High Signal Voltage	+18V ~ +3V	--
RxD Buffer	256 bytes per channel	256 bytes per channel
TxD Buffer	256 bytes per channel	256 bytes per channel
Line Impedance	--	120Ω
Input Image Size	38 Bytes	38 Bytes
Output Image Size	38 Bytes	38 Bytes
Communication Code	ASCⅡ or Hex(Binary)	ASCⅡ or Hex(Binary)
Message Length	Max. 256bytes (Start and End Character exception)	Max. 256bytes (Start and End Character exception)
Received & Transmit Start Code	STX, User setting (*default : Disable)	STX, User setting (*Default : Disable)
Received & Transmit End Code	CR, CR=User setting(*default: LF), User setting(*default: Disable)	CR, CR+User Setting (*Default: LF), User Setting(*Default: Disable)
Timeout	Range : 1~255(dec)/0.1sec~25.5sec	Range : 1~255(dec)/0.1sec~25.5sec If range is 0(dec)/0.1sec~25.5sec If range is 0(dec), disable (*default : Disable)
General Specification		
Power Dissipation	Max. 110mA @5.0Vdc	Max. 155mA @5.0Vdc
Isolation	Isolation Voltage:1000Vrms/Vac	
Field Power	Supply Voltage : 24Vdc nominal Voltage Range : 18~28.8Vdc Power Dissipation: Max. 50mA @24Vdc except Load	
Wiring	I/O Cable Max. 2.0mm² (AWG#14)	
Weight	70g	
Module Size	12mm x 99mm x 70mm	
Environment Condition	Refer to Environment Specification.	

3.2.3. Environment Specification

Environmental Specifications	
Operating Temperature	-20℃~55℃
Storage Temperature	-40℃ ~85℃
Relative Humidity	5%~90% non-condensing
Operating Altitude	2000m
Mounting	DIN rail
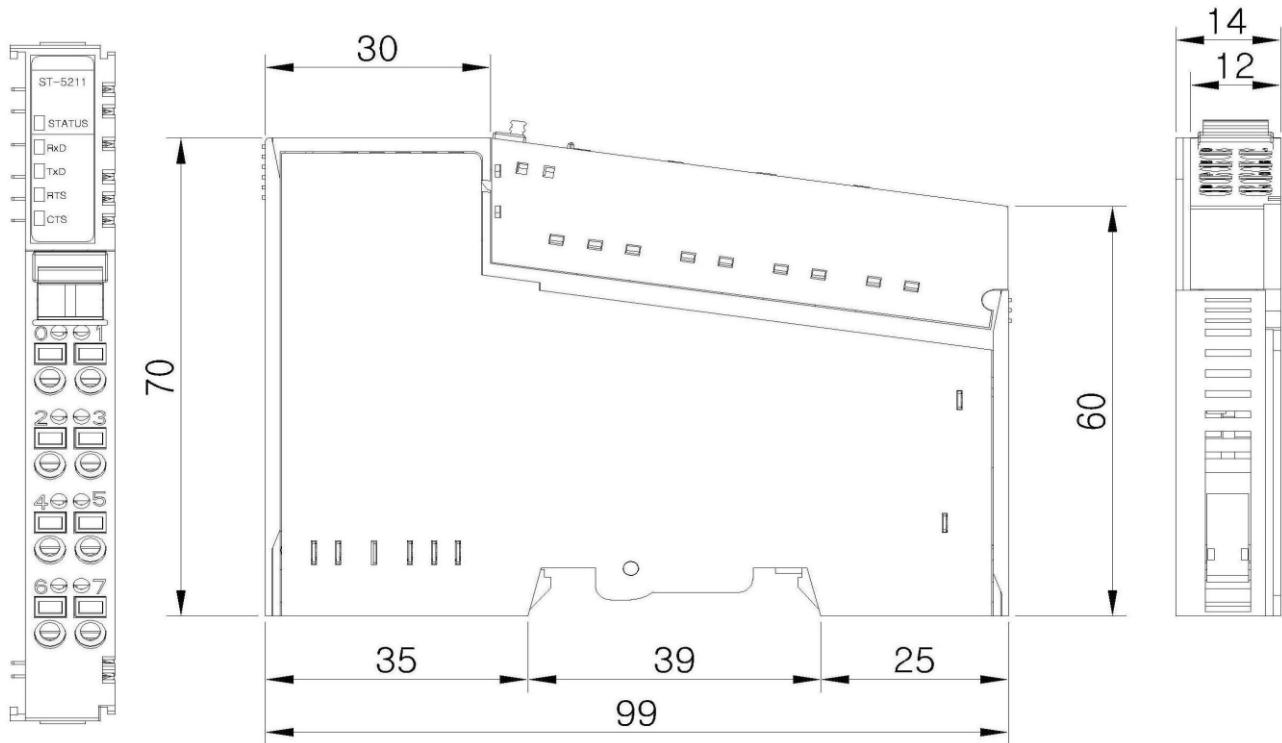
General Specifications	
Shock Operating	10g
Shock Non-Operating	30g
Vibration/Shock resistance	Displacement : 0.012Inch p-p from 10~57Hz
	Acceleration : 2G's from 57~500Hz
	Sweep Rate : 1 octave Per Minute
	Axes to test : x, y, z
	Frequency Sweeps Per Axis : 10
EMC resistance burst/ESD	EMC Directive
Installation Pos. /Protect. Class	Variable / IP20
Product Certification	CE, DNV, UL, cUL etc
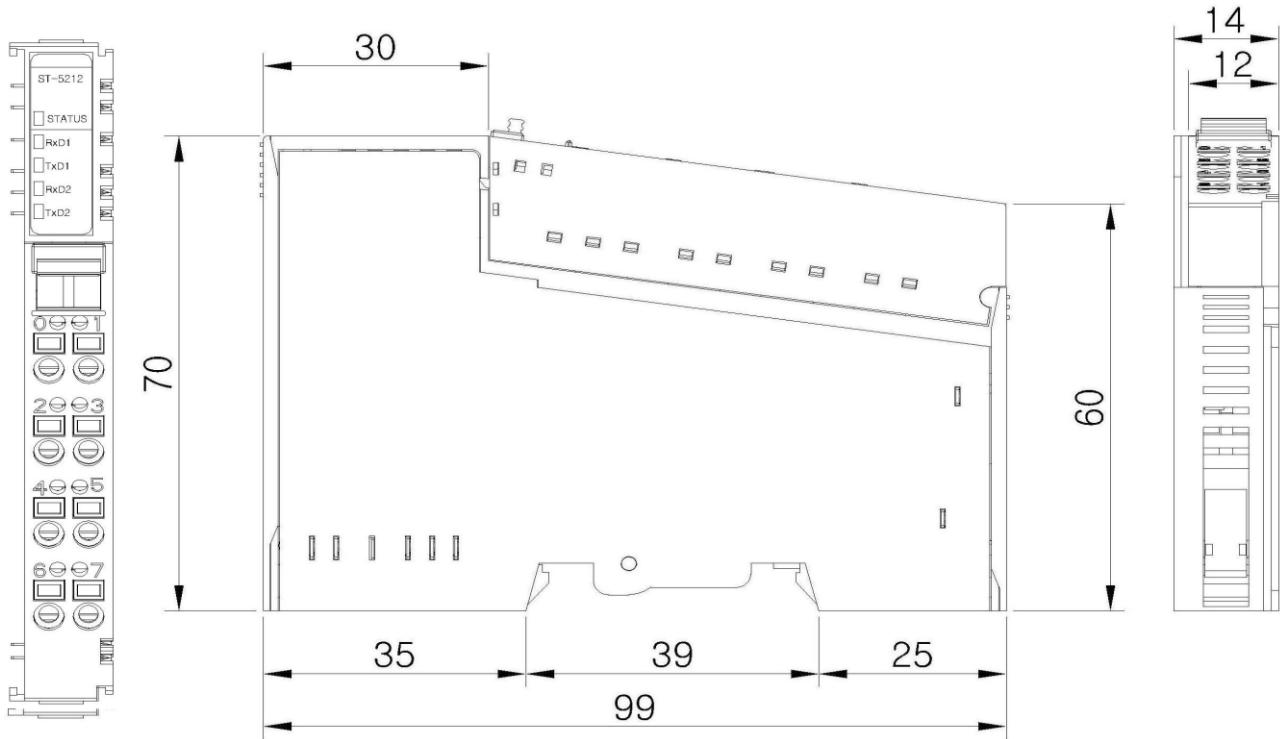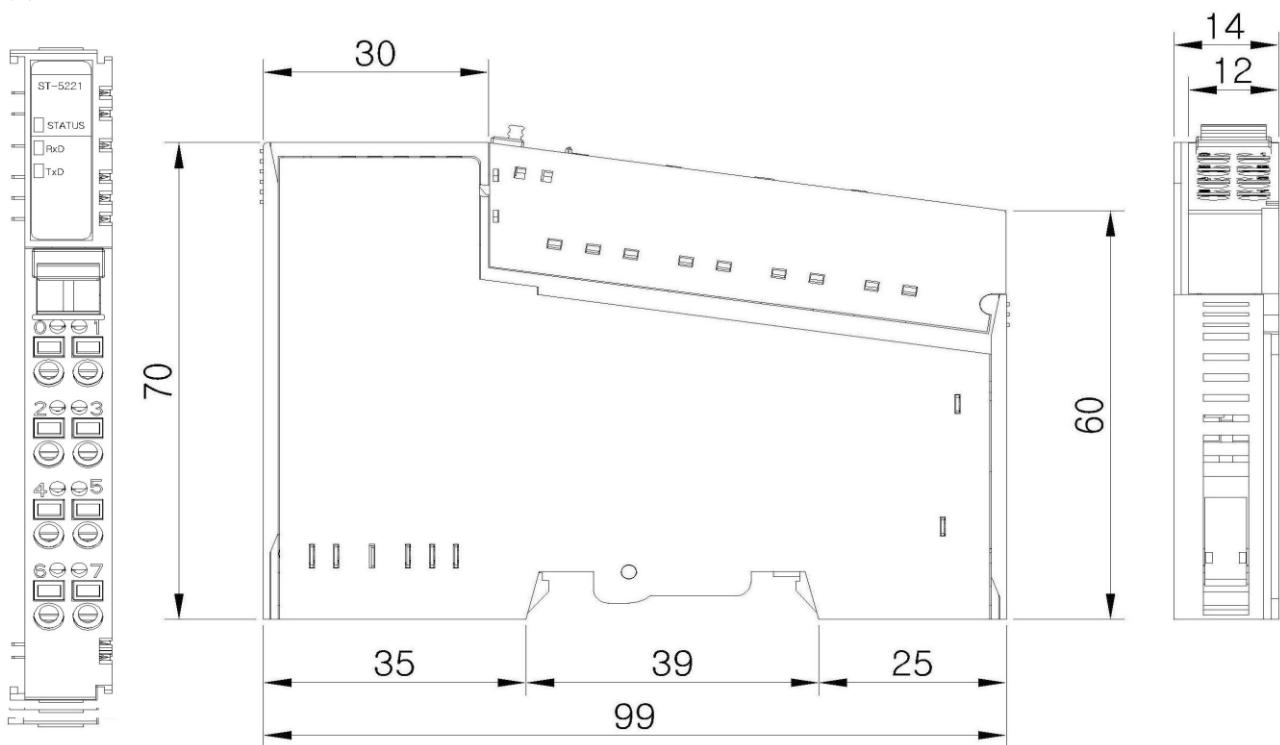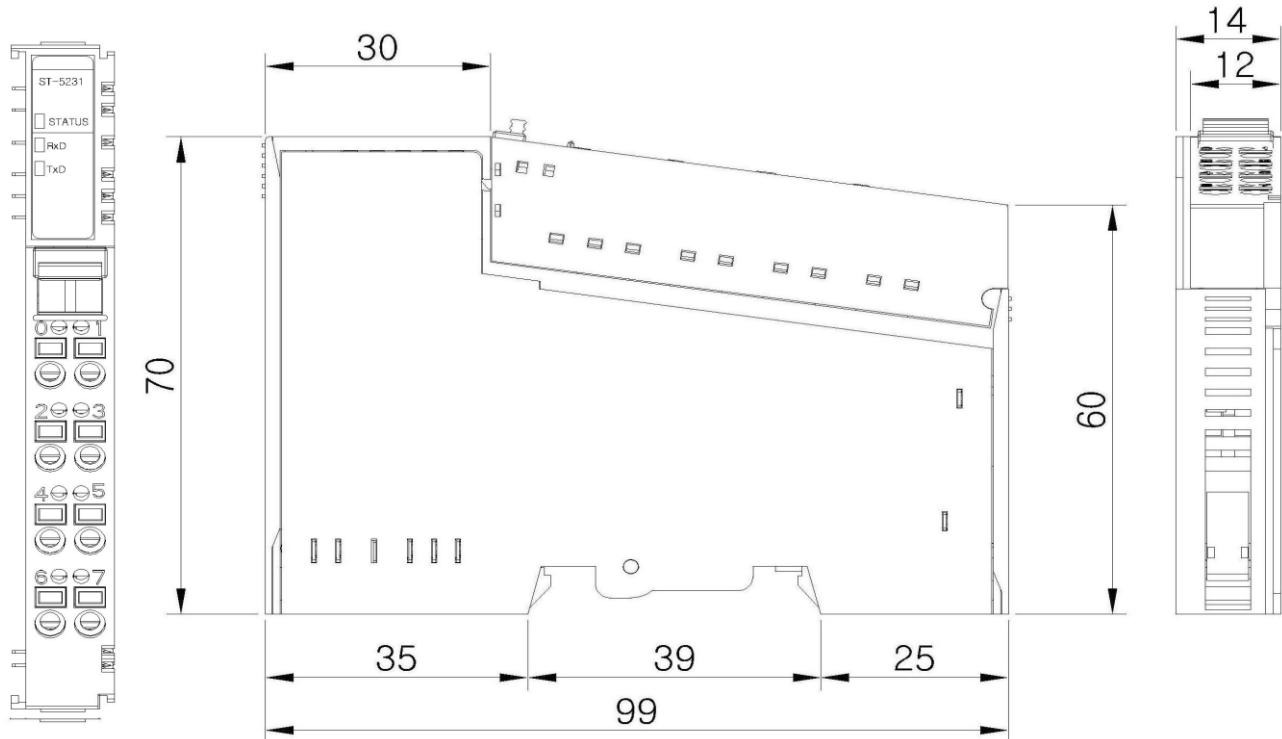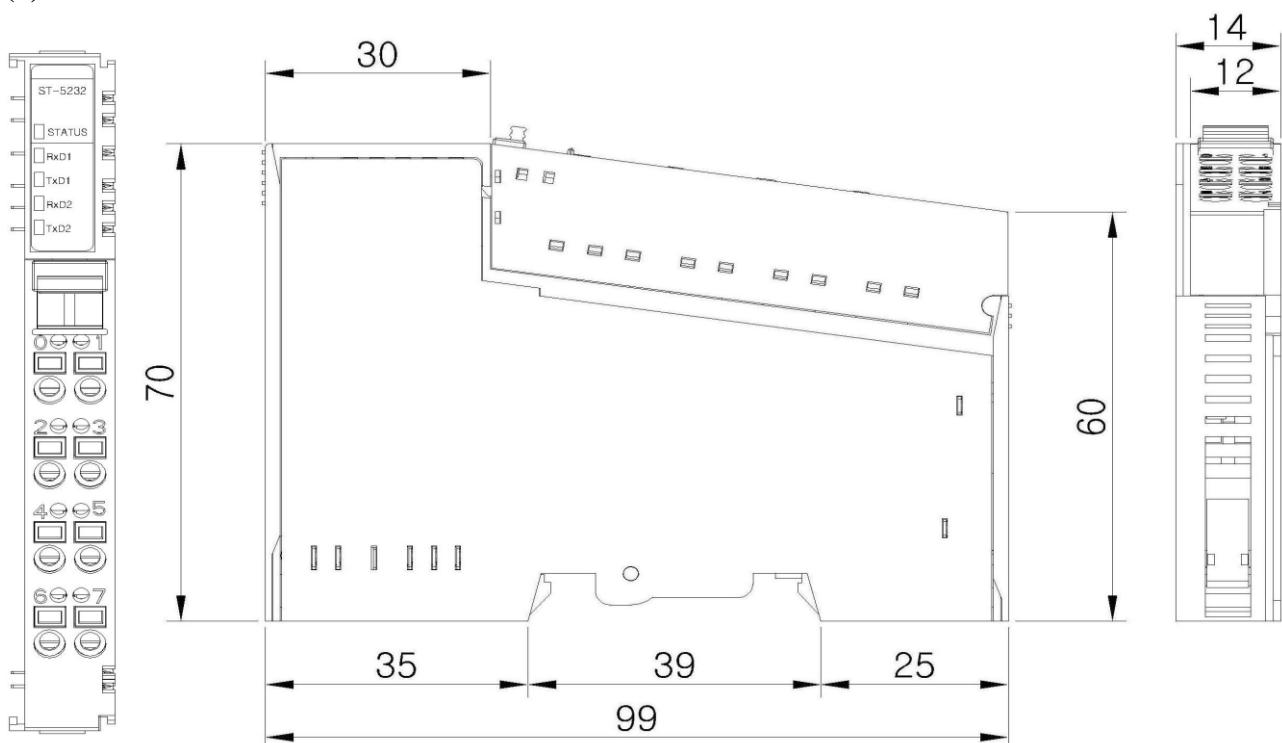
4. Dimension (mm)

4.1 ST-5211 / ST-5212 / ST-5221 / ST-5231 / ST-5232

(1)ST-5211

(2)ST-5212

(3) ST-5221

(4) ST-5231

(5) ST-5232

4.2 ST-5252, ST-5272

Coming Soon

5. Configuration and Operational Function

5.1 1-Channel Module(ST-5211, ST-5221, ST-5231)

5.1.1 Input Image Data - 6byte

Byte Offset		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
#0	STATUS Byte	TPA	IL2	IL1	IL0	RBO	RR	TA	IA
#1	Data Byte #0								
#2	Data Byte #1								
#3	Data Byte #2								
#4	Data Byte #3								
#5	Data Byte #4								

- IA : Initialization Acknowledge
- TA : Transmit Acknowledge
- RR : Receive Request
- RBO : RxD Buffer Overrun Error
  There are two counters(Run counter and Index counter) which pointing at the position of RxD Buffer Run counter is increased +1 whenever RxD inputting, Index Counter is increased as much as Input Length that brought on Input Data.
- IL : Input Length
- TPA : Transmit Processing Acknowledge
  (Related Configuration Parameter: TxD Buffering)

5.1.2 Output Image Data - 6byte

Byte Offset		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
#0	Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
#1	Data Byte #0								
#2	Data Byte #1								
#3	Data Byte #2								
#4	Data Byte #3								
#5	Data Byte #4								

- IR : Initialization Request
- TR : Transmit Request
- RA : Receive Acknowledge
- OL : Output Length
- TPR : Transmit Processing Request
  (Related Configuration Parameter: TxD Buffering)

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5.1.3 Configuration Parameter Data

Offset	Decimal Bit							
Byte #0	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
	Parity Bit 00 : No Parity 01 : Odd Parity 10 : Even Parity Others : Unused *Default : 00		Data Bit 00 : 7 Data bit 01 : 8 Data bit Others : Unused *Default : 01		Baud Rate 0000 : 300bps 0001 : 1200bps 0010: 2400bps 0011 : 4800bps 0100 : 9600bps (*Default Value) 0101 :19200bps 0110 :38400bps 0111 :57600bps 1000 : 115200bps Others : Unused			
Byte #1	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
	Reserved				CTS/RTS Flow Control 00 : RTS/CTS Disable 01 : TRS Enable 10 : CTS Enable 11 : RTS/CTS Enable *Default : 00 *Note 1		TxD Process 0 : Disable 1 : Enable *Default: 0 *Note 2	Stop Bit 0 : 1 bit 1 : 2 bit *Default: 0
Byte #2	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
	Reserved							
Byte #3	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
	Reserved							

*Note 1:

When RTS Enable, if Size of received Data is bigger than 80 %(1024 x 0.8=819) of RxD Buffer Size, RTS output actives.

*Note 2:

Disable: Transmit immediately Output Data #0~Output Data #4

Enable: Store the value of Output Data continually at RxD Buffer of Serial Interface Module, when TPA bit and TPR bit of Control Byte and Status Byte are different, transmit all Data that saved at TxD Buffer

5.2 2-Channel Module(ST-5212 and ST-5232)

5.2.1 Input Image Data - 12byte

	Byte Offset	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
#0	STATUS Byte(0ch)	TPA	IL2	IL1	IL0	RBO	RR	TA	IA
#1	Data Byte #0(0ch)								
#2	Data Byte #1(0ch)								
#3	Data Byte #2(0ch)								
#4	Data Byte #3(0ch)								
#5	Data Byte #4(0ch)								
#6	STATUS Byte(1ch)	TPA	IL2	IL1	IL0	RBO	RR	TA	IA
#7	Data Byte #0(1ch)								
#8	Data Byte #1(1ch)								
#9	Data Byte #2(1ch)								
#10	Data Byte #3(1ch)								
#11	Data Byte #4(1ch)								

- IA : Initialization Acknowledge
- TA : Transmit Acknowledge
- RR : Receive Request
- RBO : RxD Buffer Overrun Error
  There are two counters(Run counter and Index counter) which pointing at the position of RxD Buffer Run counter is increased +1 whenever RxD inputting, Index Counter is increased as much as Input Length that brought on Input Data.
- IL : Input Length
- TPA : Transmit Processing Acknowledge
  (Related Configuration Parameter: TxD Buffering)

5.2.2 Output Image Data - 12byte

Byte Offset		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
#0	Control Byte(0ch)	TPR	OL2	OL1	OL0	--	RA	TR	IR
#1	Data Byte #0(0ch)								
#2	Data Byte #1(0ch)								
#3	Data Byte #2(0ch)								
#4	Data Byte #3(0ch)								
#5	Data Byte #4(0ch)								
#0	Control Byte(1ch)	TPR	OL2	OL1	OL0	--	RA	TR	IR
#1	Data Byte #0(1ch)								
#2	Data Byte #1(1ch)								
#3	Data Byte #2(1ch)								
#4	Data Byte #3(1ch)								
#5	Data Byte #4(1ch)								

- IR : Initialization Request
- TR : Transmit Request
- RA : Receive Acknowledge
- OL : Output Length
- TPR : Transmit Processing Request
  (Related Configuration Parameter: TxD Buffering)

5.2.3 Configuration Parameter Data

Offset	Decimal Bit							
Byte #0	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
	Parity Bit 00 : No Parity 01 : Odd Parity 10 : Even Parity Others : Unused *Default : 00		Data Bit 00 : 7 Data bit 01 : 8 Data bit Others : Unused *Default : 01		Baud Rate 0000 : 300bps 0001 : 1200bps 0010: 2400bps 0011 : 4800bps 0100 : 9600bps (*Default Value) 0101 :19200bps 0110 :38400bps 0111 :57600bps 1000 : 115200bps Others : Unused			
Byte #1	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
	Reserved						TxD Process 0 : Disable 1 : Enable *Default: 0 *Note 2	Stop Bit 0 : 1 bit 1 : 2 bit *Default: 0
Byte #2	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
	Parity Bit 00 : No Parity 01 : Odd Parity 10 : Even Parity Others : Unused *Default : 00		Data Bit 00 : 7 Data bit 01 : 8 Data bit 10 : 9 Data bit Others : Unused *Default : 01		Baud Rate 0000 : 300bps 0001 : 1200bps 0010: 2400bps 0011 : 4800bps 0100 : 9600bps (*Default Value) 0101 :19200bps 0110 :38400bps 0111 :57600bps 1000 : 115200bps Others : Unused			
Byte #3	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
	Reserved						TxD Process 0 : Disable 1 : Enable *Default: 0 *Note 2	Stop Bit 0 : 1 bit 1 : 2 bit *Default: 0

*Note 2:

Disable: Transmit immediately Output Data #0~Output Data #4

Enable: Store the value of Output Data continually at RxD Buffer of Serial Interface Module, when TPA bit and
TPR bit of Control Byte and Status Byte are different, transmit all Data that saved at TxD Buffer

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5.3 2-Channel Module(ST-5252 and ST-5272)

5.3.1 Input Image Data - 38byte

Byte Offset		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
#0	Response Byte	RPST	RRCH	RRRQ	RTCH	RTBM			
#1	Input Data Length or Timeout	1-CHTO	0-CHTO	Input Data Length : 0~32 character					
#2	STATUS Byte(0ch)	TBMS	REXD	RECT	RSCT	RBOF	RBFF	RPAT	RFRM
#3	STATUS Byte(1ch)	TBMS	REXD	RECT	RSCT	RBOF	RBFF	RPAT	RFRM
#4	Incoming DL(0ch)	0~255 character							
#5	Incoming DL(1ch)	0~255 character							
#6	Input Data 00								
#7	Input Data 01								
~	~								
#36	Input Data 30								
#37	Input Data 31								

- RTBM : Return Transmit data Buffering Machines State bits.

0000 : Ready State Done	0001 : TxD Sequence 1 Done
0010 : TxD Sequence 2 Done	0011 : TxD Sequence 3 Done
0100 : TxD Sequence 4 Done	0101 : TxD Sequence 5 Done
0110 : TxD Sequence 6 Done	0111 : TxD Sequence 7 Done
1000 : TxD Sequence 8 Done	1001 : TxD Sequence 9 Done
Others : Unused	

- RTCH : Return Transmit data Channel bit.
    0:0-ch
    1:1-ch

- RRRQ : Return Received data Request bit.

- RRCH : Return Received data Channel bit.
    0:0-ch
    1:1-ch

- RPST : Return Preset bit.

- 0-CHTO and 1-CHTO : 0-Channel Timeout and 1-Channel Timeout.

- RFRM : FRAMING ERROR

- RPAT : PARITY ERROR

- RBFF : RxD Buffer Full(RxBuffer Size-256Byte)

* In case Fixed Length Mode, RxBuffer Size = Fixed Length Value

- RBOF : RxD Buffer Overflow(RxBuffer Size > 256Byte)

* In case Fixed Length Mode, Rxbuffer Size > Fixed Length Value

- RSCT : Found Start Character of RxD

- RECT : Found End Character of RxD

- REXD : Exist RxData in RxD Buffer

- TBMS : TxBuffering Machine State Error

5.3.2 Output Image Data - 38byte

Byte Offset		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
#0	Response Byte	CPST	CRCH	CRRQ	CTCH	CTBM			
#1	Output Data Length	Output Data Length : 0~32 character							
#2	-	Reserved							
#3	-	Reserved							
#4	-	Reserved							
#5	-	Reserved							
#6	Output Data 00								
#7	Output Data 01								
~	~								
#36	Output Data 30								
#37	Output Data 31								

- CTBM : Control Transmit data Buffering Machine State bits.
  - 0000 : TxD Ready State   0001 : TxD Sequence 1
  - 0010 : TxD Sequence 2   0011 : TxD Sequence 3
  - 0100 : TxD Sequence 4   0101 : TxD Sequence 5
  - 0110 : TxD Sequence 6   0111 : TxD Sequence 7
  - 1000 : TxD Sequence 8(Buffering after Send)   1001 : TxD Sequence 9(Buffering after Send)
  - Others : Error(TBMS=1)

- CTCH : Control Transmit data Channel bit.
  - 0:0-ch
  - 1:1-ch

- CPRQ : Control Received data Request bit.
  - 0:0-ch
  - 1:1-ch

- CRCH : Control Received data Channel bit.

- CPST : Control Preset bit

5.3.3 Configuration Parameter Data

Offset	Decimal Bit							
Byte #00	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	0-ch Stop Bit 0: 1bit 1: 2bit (*default : 0)	0-ch Parity Bit 00:No Parity(*default) 01:Odd Parity 10:Even Parity Others: Unused		0-ch Data bit 00: 7 Data Bit 01: 8 Data Bit(*default) Others: Unused		0-ch Baud Rate 000 : 1200bps 001 : 2400bps 010 : 4800bps 011 : 9600bps (*default) 100 : 19200bps 101 : 38400bps 110 : 57600bps 111 : 115200bps		
Byte #01	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	1-ch Stop Bit 0: 1bit 1: 2bit (*default : 0)	1-ch Parity Bit 00: No Parity(*default) 01: Odd Parity 10: Even Parity Others: Unused		1-ch Data bit 00 : 7 Data Bit 01 : 8 Data Bit(*default) Others: Unused		1-ch Baud Rate 000 : 1200bps 001 : 2400bps 010 : 4800bps 011 : 9600bps (*default) 100 : 19200bps 101 : 38400bps 110 : 57600bps 111 : 115200bps		
Byte #02	0- Channel (Set Parameter about Start and end Character)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	TxD End Character 00 : Disable(*default) 01 : TxD 1-E/C 10 : TxD 2-E/C 11 : Reserved(Disable)		TxD Start Character 00 : Disable(*default) 01 : TxD 1-S/C 10 : TxD 2-S/C 11 : Reserved(Disable)		RxD End Character 00 : Disable(*default) 01 : RxD 1-E/C 10 : RxD 2-E/C 11 : Reserved(Disable)		RxD Start Character 00 : Disable(*default) 01 : RxD 1-S/C 10 : RxD 2-S/C 11 : Reserved(Disable)	
Byte #03	1- Channel (Set Parameter about Start and end Character)							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	TxD End Character 00 : Disable(*default) 01 : TxD 1-E/C 10 : TxD 2-E/C 11 : Reserved(Disable)		TxD Start Character 00 : Disable(*default) 01 : TxD 1-S/C 10 : TxD 2-S/C 11 : Reserved(Disable)		RxD End Character 00 : Disable(*default) 01 : RxD 1-E/C 10 : RxD 2-E/C 11 : Reserved(Disable)		RxD Start Character 00 : Disable(*default) 01 : RxD 1-S/C 10 : RxD 2-S/C 11 : Reserved(Disable)	
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Byte #04	0-ch RxD 1-S/C (*default : 0x00)							
Byte #05	0-ch RxD 2-S/C (*default : 0x00)							
Byte #06	0-ch RxD 1-E/C (*default : 0x00)							
Byte #07	0-ch RxD 2-E/C (*default : 0x00)							
Byte #08	0-ch TxD 1-S/C (*default : 0x00)							
Byte #09	0-ch TxD 2-S/C (*default : 0x00)							
Byte #10	0-ch TxD 1-E/C (*default : 0x00)							
Byte #11	0-ch TxD 2-E/C (*default : 0x00)							
Byte #12	1-ch RxD 1-S/C (*default : 0x00)							
Byte #13	1-ch RxD 2-S/C (*default : 0x00)							

Byte #14	1-ch RxD 1-E/C (*default : 0x00)
Byte #15	1-ch RxD 2-E/C (*default : 0x00)
Byte #16	1-ch TxD 1-S/C (*default : 0x00)
Byte #17	1-ch TxD 2-E/C (*default : 0x00)
Byte #18	1-ch TxD 1-E/C (*default : 0x00)
Byte #19	1-ch TxD 2-E/C (*default : 0x00)
Byte #20	0-Channel Fixed Length Function 0x00 : F/L Mode Disable(*default) 0x01 ~ 0xFF : F/L Mode Enable and Fixed Length Value
Byte #21	1-Channel Fixed Length Function 0x00 : F/L Mode Disable(*default) 0x01 ~ 0xFF : F/L Mode Enable and Fixed Length Value
Byte #22	0-Ch Timeout Value Setting 0(dec) : Timeout Disable 1(dec) : 100ms 50(dec) : 5,000ms(5sec) *default 100(dec) : 10,000ms(10sec) 200(dec) : 20,000ms(20sec) 255(dec) : 25,500ms(25.5sec)
Byte #23	1-Ch Timeout Value Setting 0(dec) : Timeout Disable 1(dec) : 100ms 50(dec) : 5,000ms(5sec) *default 100(dec) : 10,000ms(10sec) 200(dec) : 20,000ms(20sec) 255(dec) : 25,500ms(25.5sec)

- S/C : Start Character

- E/C : End Character

- F/L : Fixed Length

6. Initialization of the Module

6.1 Control Byte

- ✓ Set Bit in control byte to '1'
- ✓ Receive and Transmit functions are stopped.
- ✓ RxD Buffer and TxD Buffer are erased.
- ✓ Serial Interface Module will set configuration parameter value.

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	x	x	x	x	x	x	x	IR

6.2 Status Byte

- ✓ If IA in Status Byte set to '1', Initialization of serial interface module success.

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	x	x	x	x	x	x	x	IA

7. EXAMPLE

7.1 Example of Transmitting data (Transmit Data "CREVIS.CO.KR")

- Step #0

TR inverting (TR≠TA)
Output Length = 5
Output Data = "CREVI"

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	x	x	x	x	x	x	0	0

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	1	0	1	x	x	1	0
Output Byte #0	'C'(0x43 :ASCII code)
Output Byte #1	'R'(0x52)
Output Byte #2	'E'(0x45)
Output Byte #3	'V'(0x56)
Output Byte #4	'I'(0x49)

- Step #1

Check TA bit value in Status Byte.
TR=TA: transmit complete.

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	x	x	x	x	x	x	1	0

- Step #2

TR inverting (TR≠TA)
Output Length = 5
Output Data = "S.CO."

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	1	0	1	x	x	0	0
Output Byte #0	'S'(0x53)
Output Byte #1	'.'(0x2E)
Output Byte #2	'C'(0x43)
Output Byte #3	'O'(0x4F)
Output Byte #4	'.'(0x2E)

- Step #3

Check TA bit value in Status Byte.

TR=TA: transmit complete.

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	x	x	x	x	x	x	0	0

- Step #4

TR inverting (TR≠TA)

Output Length = 2

Output Data = "KR"

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	0	1	0	x	x	1	0
Output Byte #0	'K'(0x4B)							
Output Byte #1	'R'(0x52)							
Output Byte #2								
Output Byte #3								
Output Byte #4								

- Step #5

Check TA bit value in Status Byte.

TR=TA: transmit complete.

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	x	x	x	x	x	x	1	0

CREVIS

7.2 Example of Receiving data (Receive Data "Welcome")

- Step #0

RR=RA

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	x	x	x	x	x	0	x	0

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	x	x	x	x	0	x	0

- Step #1

RA inverting (RA≠RR)

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	x	x	x	x	1	x	0

- Step #2

RA inverting (RA=RR)
Input Length = 5
Input Data = "Welco"

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	1	0	1	x	1	x	0
Input Byte #0	'W'(0x57)							
Input Byte #1	'e'(0x65)							
Input Byte #2	'l'(0x6C)							
Input Byte #3	'c'(0x63)							
Input Byte #4	'o'(0x6F)							

- Step #3

RA inverting (RA≠RR)

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	x	x	x	x	0	x	0

- Step #4

RA inverting (RA=RR)

Input Length = 2

Input Data = "me"

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	0	1	0	x	0	x	0
Input Byte #0	'm'(0x6D)							
Input Byte #1	'e'(0x65)							
Input Byte #2	0x00							
Input Byte #3	0x00							
Input Byte #4	0x00							

CREVIS

7.3 Example of Transmitting data and Receiving data

(Transmit: "Welcome", Receive: "Welcome")

- Step #0 (Transmit)

TR inverting (TR≠TA)

Output Length = 5

Output Data = "Welco"

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	1	0	1	x	x	1	0
Output Byte #0	'W'(0x57)							
Output Byte #1	'e'(0x65)							
Output Byte #2	'l'(0x6C)							
Output Byte #3	'c'(0x63)							
Output Byte #4	'o'(0x6F)							

- Step #1

Check TA bit value in Status Byte.

TR=TA: transmit complete**.**

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	x	x	x	x	x	x	1	0

- Step #2

TR inverting (TR≠TA)

Output Length = 2

Output Data = "me"

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	0	1	0	x	x	0	0
Output Byte #0	'm'(0x6D)							
Output Byte #1	'e'(0x65)							
Output Byte #2								
Output Byte #3								
Output Byte #4								

- **Step #3**

Check TA bit value in Status Byte.
TR=TA: transmit complete.

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	x	x	x	x	x	x	0	0

- **Step #4 (Receive)**

Check (RR=RA)

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	x	x	x	x	x	0	x	0

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	x	x	x	x	0	x	0

- **Step #5**

RA inverting (RA≠RR)

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	x	x	x	x	1	x	0

- **Step #6**

RA inverting (RA=RR)
Input Length = 5

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	1	0	1	x	1	x	0

Check Input Data = "Welco"

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	1	0	1	x	1	x	0
Input Byte #0	W							
Input Byte #1	e							
Input Byte #2	l							
Input Byte #3	c							
Input Byte #4	o							

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- **Step #7**

RA inverting (RA≠RR)

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	x	x	x	x	0	x	0

- **Step #8**

RA inverting (RA=RR)

Input Length = 2

Check Input Data = "me"

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	x	0	1	0	x	0	x	0
Input Byte #0	'm'							
Input Byte #1	'e'							
Input Byte #2								
Input Byte #3								
Input Byte #4								

7.4 TPR and TPA Example ("Welcome")

- Step #0

TxD Process data in Configuration Parameter set to "1" (Enable)

- Step #1

RA inverting (RA≠RR)
Output Length = 5
Output Data = "Welco"

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	0	x	x	x	x	x	0	0
	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	0	1	0	1	x	x	1	0
Output Byte #0	'W'(0x57)							
Output Byte #1	'e'(0x65)							
Output Byte #2	'l'(0x6C)							
Output Byte #3	'c'(0x63)							
Output Byte #4	'o'(0x6F)							

- **Step #2**

Check TA bit value in Status Byte.

TR=TA: transmit complete.

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	0	x	x	x	x	x	1	0

TxD Buffer

Offset	TxD Buffer Data
0	W(0x57)
1	e(0x65)
2	l(0x6C)
3	c(0x63)
4	o(0x6F)
5	
6	
7	
8	
:	:
:	:
:	:
253	
254	
255	

- **Step #3**

RA inverting (RA≠RR)

Output Length = 2

Output Data = "me"

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	0	0	1	0	x	x	0	0
Output Byte #0	'm'(0x6D)							
Output Byte #1	'e'(0x65)							
Output Byte #2								
Output Byte #3								
Output Byte #4								

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- Step #4

Check TA bit value in Status Byte.

TR=TA: transmit complete

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	0	x	x	x	x	x	0	0

TxD Buffer

Offset	TxD Buffer Data
0	W(0x57)
1	e(0x65)
2	l(0x6C)
3	c(0x63)
4	o(0x6F)
5	m(0x5D)
6	e(0x65)
7	
8	
:	:
:	:
:	:
253	
254	
255	

- **Step #5**

TPR inverting (TPR≠TPA)

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Control Byte	TPR	OL2	OL1	OL0	--	RA	TR	IR
	1	0	1	0	x	x	0	0

Transmit all TxD Buffer data (TxD Buffer empty)

Offset	TxD Buffer Data
0	
1	
2	
3	
4	
5	
6	
7	
8	
:	:
:	:
:	:
253	
254	
255	

- **Step #6**

Check TPA bit value in Status Byte.

TPR=TPA: transmit complete

	7bit	6bit	5 bit	4 bit	3 bit	2 bit	1 bit	0 bit
Status Byte	TPA	IL2	IL1	IL0	OR	RR	TA	IA
	1	x	x	x	x	x	0	0

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8. Trouble Shooting

ATTENTION	In this manual, it couldn't be described all variety case with Network Adapter of several protocols. So if you couldn't find any fault after investigating all below cases, refer to NA user manual.

LED Status	Cause	Action
All LED turns off	- No power	- Check main power Cable
	- System power is not supplied.	- Contact Sales team and send module for repair.
STATUS LED flashes red	- Excess of expansion slot - Excess of IO size - Wrong IO composition - Occurrence of EEPROM checksum error	- Use expansion slot up to 32. - Compose that IO total size is not excess. - Check composition I/O Module